STK8321-W

Digital Output 3-axis MEMS Accelerometer

Datasheet

Version – 1.5

2022/02/10

Hazardous Substance Free

RoHS / REACH Compliant

Sensortek Technology Corporation

1. OVERVIEW

Description

The STK8321-W is a ±2g/±4g/±8g, 3-axis linear accelerometer, with digital output (I^2C and SPI). It is a low-profile capacitive MEMS sensor featuring, compensation for 0g offset and gain errors, and conversion to 12-bit digital values at user configurable samples per second. The device can be arranged for sensor data changes through the interrupt pins. The STK8321-W is available in a small 2.0mm x 2.0mm x 1.0 mm LGA package and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Feature

- Low Voltage Operation:
  - Supply Internal Domain Voltage: 1.7V~3.6V
  - I/O Voltage Range: 1.62V~3.6V
- ±2g/±4g/±8g dynamically selectable full-scale
- I^2C digital output interface
- 3-wire and 4-wire SPI digital output
- 2 physical interrupts
- Low noise
- 12-bit data output
- 10000 g high shock survivability
- 2.0mm x 2.0mm x 1.0 mm LGA Package
- Configurable Samples from 14 to 2000 samples per second
- Sleep Feature for Low Power Consumption
- On-chip interrupt controller, motion-triggered interrupt-signal generation for
  - New data
  - Any-motion (slope) detection
  - Significant motion
- On-chip FIFO, integrated 32 frames FIFO buffer
- RoHS Compliant
- Halogen Free
- Environmentally Preferred Product
- Moisture Sensitivity Level 3

Applications

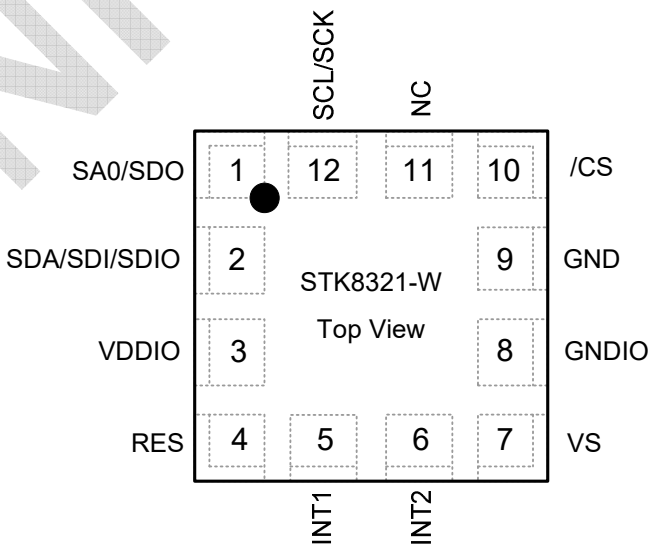
- Display orientation
- Gaming and virtual reality input devices
- Impact recognition and logging
- Vibration monitoring and compensation
- Pedometer
- Activity trackers for fitness apps
- Smart power management for mobile devices

2. PIN DESCRIPTION

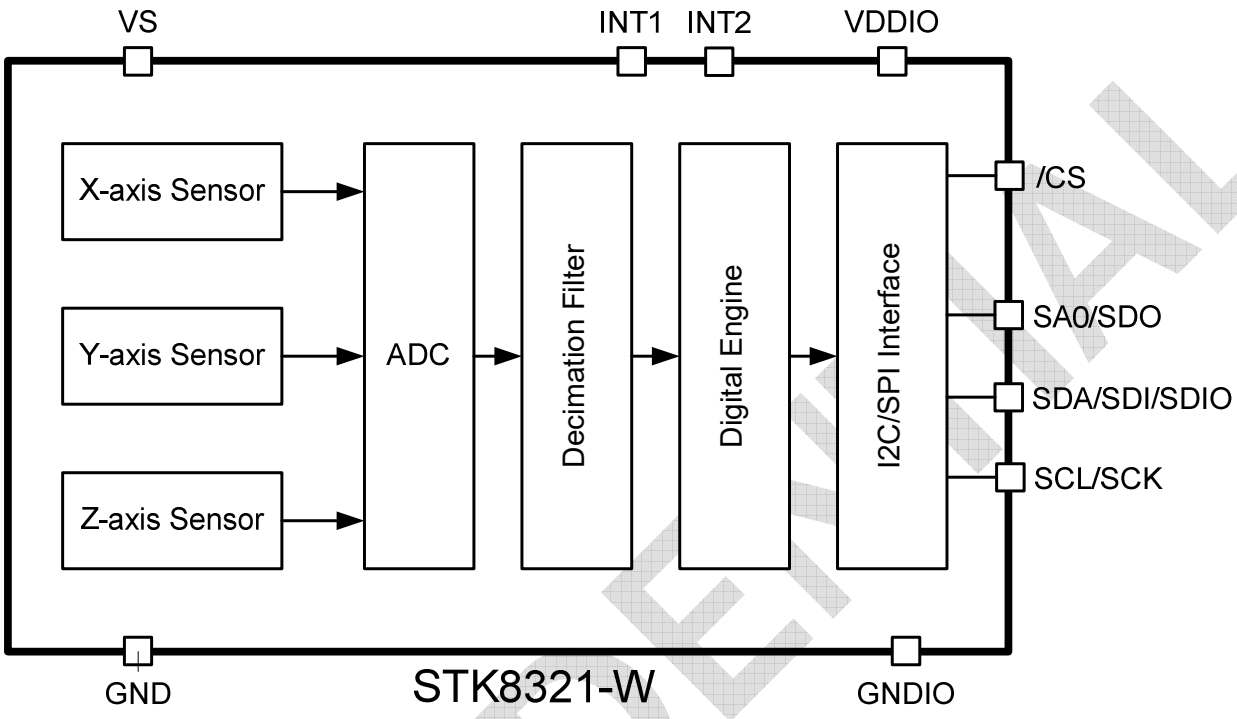
Pin#	Name	Dir.	Function
1	SA0/SDO	I	I^2C slave address selection pin, '1' for 0x1F and '0' for 0x0F. Serial Data Output (SPI 4-Wire)/ NC (SPI 3-Wire).
2	SDA/SDI/SDIO	B	Serial Data (I^2C, Open-Drain). Serial Data Input (SPI 4-Wire). Serial Data Input and Output (SPI 3-Wire).
3	VDDIO	PWR	Digital Interface Supply Voltage.
4	Reserved	I	Recommended tie to GND.
5	INT1	O	Interrupt 1 Output.
6	INT2	O	Interrupt 2 Output.
7	VS	PWR	Supply Voltage.
8	GNDIO	GND	Must be connected to ground.
9	GND	GND	Must be connected to ground.
10	/CS	I	'0' for SPI mode. '1' or floating for I2C mode. SPI mode Chip Select.
11	NC	NC	Not Internally Connected.
12	SCL/SCK	I	Serial Communications Clock (I^2C, Open-Drain).

Direction denotation

O	Output	GND	Ground
I	Input	B	Bi-direction
PWR	Power	NC	Not Connected



3. FUNCTION BLOCK



4. ELECTRICAL SPECIFICATIONS

T_A = 25°C, VS = 2.6 V, VDDIO = 2.6 V, acceleration = 0 *g*, C_S = $C_{I/O}$ = 10 µF and 0.1 µF

Parameter	Test Conditions	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Voltage Range (VS)		1.7	1.8	3.6	V
Interface Voltage Range (VDDIO)		1.62	1.8	3.6	V
Current consumption in normal mode			110		µA
Current consumption in suspend mode			1		µA
Current consumption in low-power mode	Sleep duration=25 ms Bandwidth=1k Hz		7		uA
Digital high level input voltage (VIH)		0.7 x VDDIO			V
Digital low level input voltage (VIL)				0.3 x VDDIO	V
High level output voltage (VOH)[1]		0.8 x VDDIO			V
Low level output voltage (VOL)[1]				0.2 x VDDIO	V
OUTPUT DATA RATE AND BANDWIDTH	Each axis				
Bandwidth (BW)			7.81		Hz
			15.63		Hz
			31.25		Hz
			62.5		Hz
			125		Hz
			250		Hz
			500		Hz
			1000		Hz
Output data rate (ODR) in normal mode			BW * 2		Hz

1. IOL = 10mA, IOH = -4mA

5. MECHANICAL SPECIFICATIONS

T_A = 25°C, VS = 2.6 V, VDDIO = 2.6 V, acceleration = 0 *g*, C_S = $C_{I/O}$ = 10 µF and 0.1 µF

Parameter	Test Conditions	Min	Typical	Max	Unit
SENSOR INPUT	Each axis				
Measurement Range	User selectable		±2, ±4, ±8		g
Non-linearity	Percentage of full scale		±0.5		%FS
Cross-Axis Sensitivity			1		%
OUTPUT RESOLUTION	Each axis				
±2 g Range	Full resolution		12		Bits
±4 g Range	Full resolution		12		Bits
±8 g Range	Full resolution		12		Bits
SENSITIVITY	Each axis				
Sensitivity at XOUT, YOUT, ZOUT	±2g, 12-bit resolution		1024		LSB/g
	±4g, 12-bit resolution		512		LSB/g
	±8g, 12-bit resolution		256		LSB/g
Sensitivity Change Due to Temperature	X-, Y-, Z-Axes		±0.02		%/°C
0 g OFFSET[1]	Each axis				
0 g Output for XOUT, YOUT, ZOUT			±100		mg
0 g Offset Change Due to Temperature	X-, Y-, Z-Axes		±1		mg/°C
NOISE					
X-, Y-, Z-Axes	±2g, 12-bit resolution BW = 62.5 Hz		300		µg/sqrt(Hz)

1. These parameters are tested in production at final test, and could slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress.

6. ABSOLUTE MAXIMUM RATINGS

Symbol	Ratings	Maximum value	Unit
VS	Supply voltage	-0.3 to 3.6	V
VDDIO	Digital Interface Supply Voltage	-0.3 to 3.6	V
Vin	Input voltage on any control pin	-0.3 to 3.6	V
A_{UNP}	Acceleration (any axis, unpowered)	10000	g
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV
		500 (CDM)	V
		200 (MM)	V
		100 (Latch Up)	mA

7. DIGITAL INTERFACE

Both I²C and SPI digital interface are available in STK8321-W. In both cases, the STK8321-W operates as a slave device. /CS (chip select) pin state is used to select the operation interface. The I²C mode is enabled if the /CS pin is tied high to VDDIO. And the SPI mode is enabled when the /CS pin is tied to low.

7.1 I²C

All registers in STK8321-W can be accessed via the I²C bus. All operations can be controlled by the related registers. There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional signal used for sending and receiving the data to/from the interface. Both signals are pull-up to $V_{DD\ I/O}$ through an external resistor.

The Slave Address associated to the STK8321-W is 0x0F or 0x1F which is modified by the ADDSEL pin. If the ADDSEL pin is connected to the VDDIO, the address is 0x1F, otherwise if the ADDSEL pin is connected to ground, the address is 0x0F. This solution permits to connect and address two different accelerometers to the same I²C lines.

A watchdog timer (WDT) is used to prevent the I²C bus lock-up by STK8321-W. The I²C bus will be reset and return to normal operation state once the WDT is reached. The WDT can be enabled/disabled by I2C_WDT_EN bit and the timer period can be set by I2C_WDT_SEL bit in register INTFCFG(0x34)

The STK8321-W I²C command format description for reading and writing operation between the host and STK8321-W are shown in the following timing chart.

Slave Address

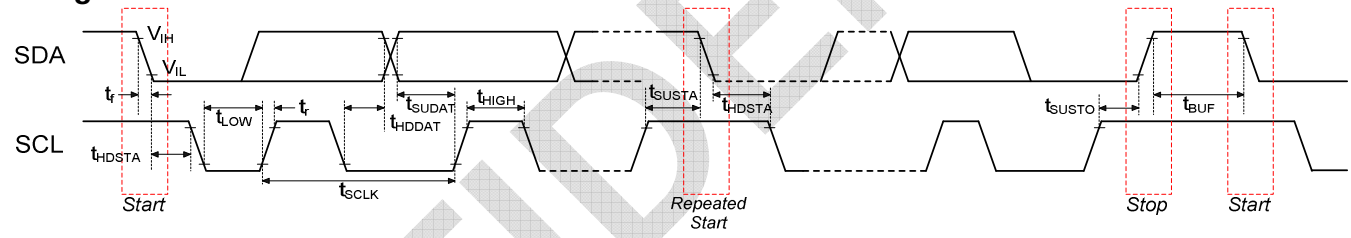
/CS pin	SA0 pin	Slave Address (7-bit)	R/W Command Bit	OPERATION
1 or float	1	0x1F	0	Write Data to STK8321-W
			1	Read Data form STK8321-W
	0	0x0F	0	Write Data to STK8321-W
			1	Read Data form STK8321-W

Characteristics of the I²C Timing

Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
f_{SCLK}	SCL clock frequency	10	100	10	400	kHz
t_{HDSTA}	Hold time after (repeated) start condition. After this period, the first clock is generated	4.0	—	0.6	—	μs
t_{LOW}	LOW period of the SCL clock	4.7	—	1.3	—	μs
t_{HIGH}	HIGH period of the SCL clock	4.0	—	0.6	—	μs
t_{SUSTA}	Set-up time for a repeated START condition	4.7	—	0.6	—	μs
t_{HDDAT}	Data hold time	0	—	0	—	ns
t_{SUDAT}	Data set-up time	250	—	100	—	ns
t_r	Rise time of both SDA and SCL signals	—	1000	—	300	ns
t_f	Fall time of both SDA and SCL signals	—	300	—	300	ns
t_{SUSTO}	Set-up time for STOP condition	4.0	—	0.6	—	μs
t_{BUF}	Bus free time between a STOP and START condition	4.7	—	1.3	—	μs

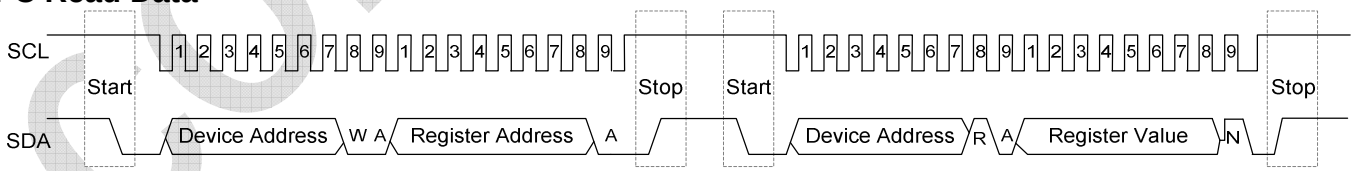
Note: f_{SCLK} is the $(t_{SCLK})^{-1}$.

Timing Chart of the I²C

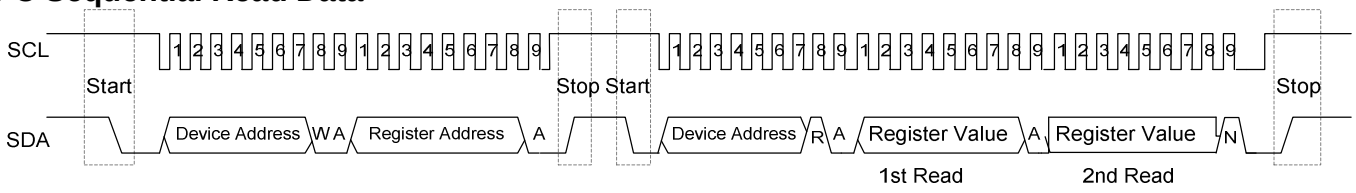


I²C Write Command

I²C Read Data



I²C Sequential Read Data

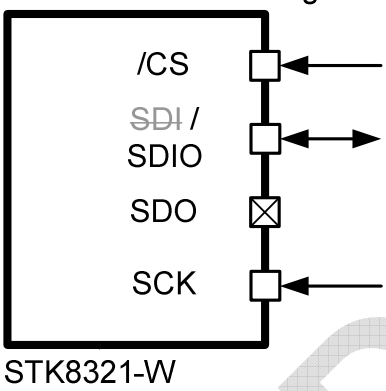


7.2 SPI

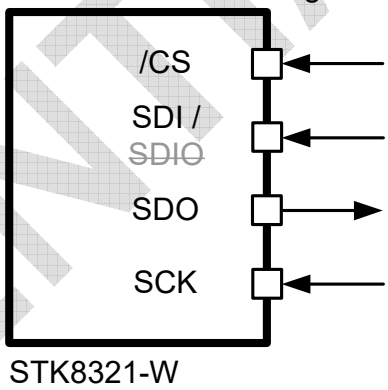
For SPI, either 3- or 4-wire configuration is possible. The STK8321-W is also compatible with '00' (mode 0) and '11' (mode 3) SPI mode. The automatic selection between '00' [CPOL = 0 and CPHA = 0] and '11' [CPOL = 1 and CPHA = 1] is done based on the SCK value at the falling edge of /CS.

The 3-or 4-wire SPI connection diagram are shown below. The maximum SPI clock speed is 8MHz with 25pF maximum loading. The 3-wire SPI can be selected by setting SPI_3WM bit in INTFCFG (0x34) to 1. When using 3-wire SPI, it is recommended that the SDO pin either be pulled up to VDDIO or be pulled down to GND via a 10 kΩ resistor.

3- Wire SPI Connection Diagram



4- Wire SPI Connection Diagram

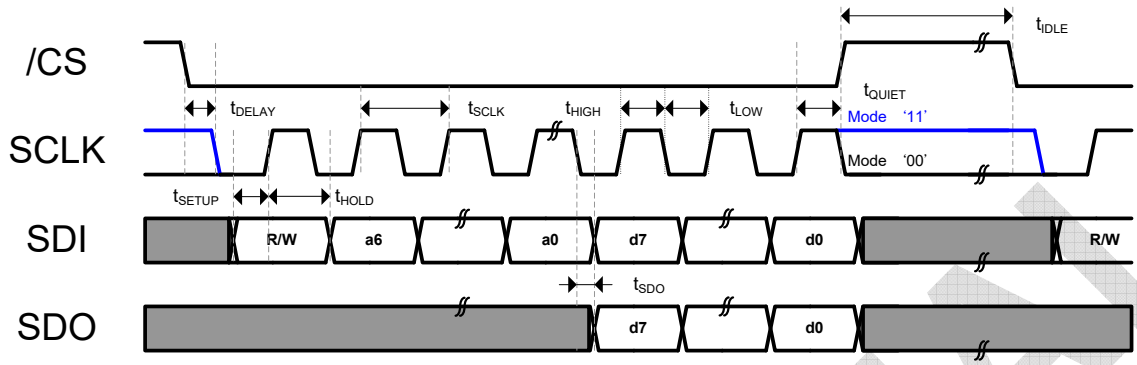


The timing diagram for 3-wire and 4-wire SPI reads or writes is shown in the following figure.

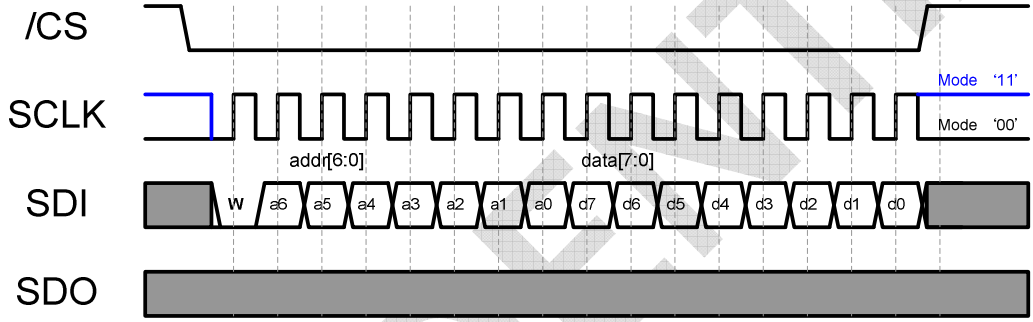
Characteristics of the SPI Timing

Symbol	Parameter	Condition	Min.	Max.	Unit
f_{SCLK}	SPI clock frequency.			8	MHz
t_{SCLK}	1/ f_{SCLK}		125	—	ns
t_{HIGH}	SCLK high pulse width.		62.5		ns
t_{LOW}	SCLK low pulse width.		62.5		ns
t_{DELAY}	/CS falling edge to SCLK falling edge.		30	—	ns
t_{QUITE}	SCLK rising edge to /CS rising edge		70	—	ns
t_{SETUP}	Set-up time for SDI		20	—	ns
t_{HOLD}	Hold time for SDI		20	—	ns
t_{SDO}	SDO output delay.	VDDIO > 2.2V	—	30	ns
		VDDIO ≤ 2.2V		40	ns
t_{IDLE}	SPI bus idle time between two success bus transactions.		20	—	ns

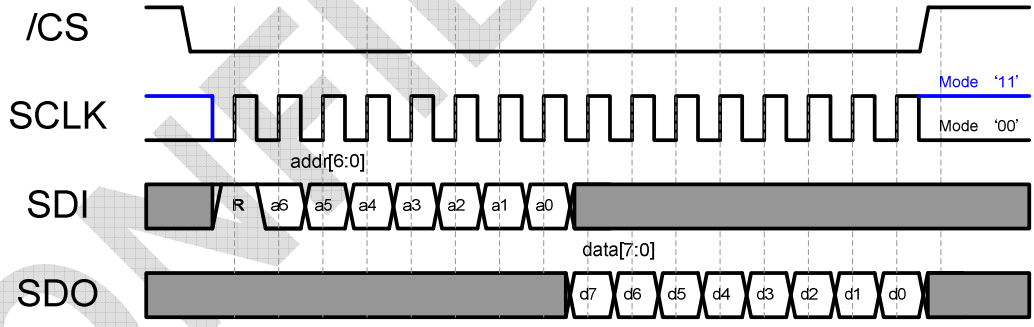
Timing Chart of the SPI



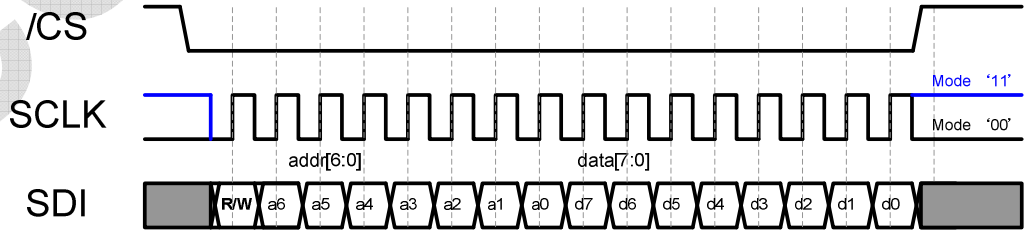
SPI 4-Wire Write Command



SPI 4-Wire Read Data



SPI 3-Wire Read/Write



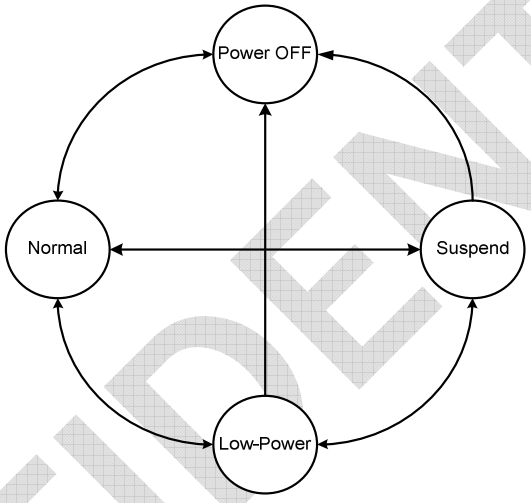
8. PRINPICLE OF OPERATION

8.1 Mode of Operation

STK8321-W acts as a slave and can communicate with a master (uC or uP). Acceleration data and status information can be accessed with I²C or SPI interface. The interrupt pin are freely configured by user, depends on different requirements.

8.2 Power Management

STK8321-W has three different power modes, Normal Mode, Low-Power Mode and Suspend Mode. After power-on, it will enter Normal Mode, and user can transfer to Low-Power Mode or Suspend Mode for power-saving purpose.

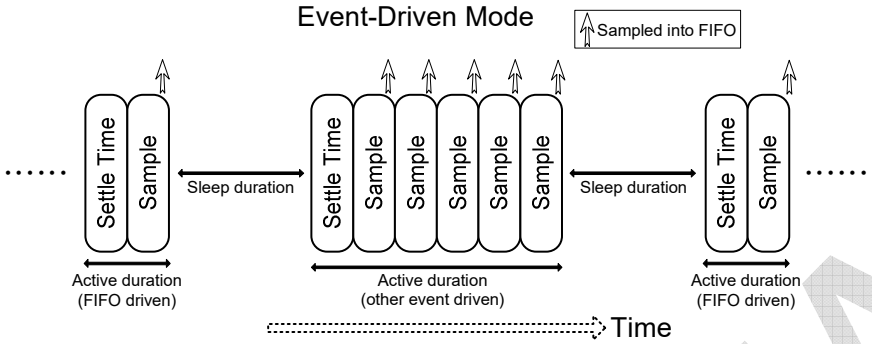


In **Normal Mode**, all functions are available and data acquisition is performed continuously. Changing register values at this mode is not recommended. Please set STK8321-W registers after entering suspend mode. Once the user confirms the settings, switch back to normal mode to enable STK8321-W.

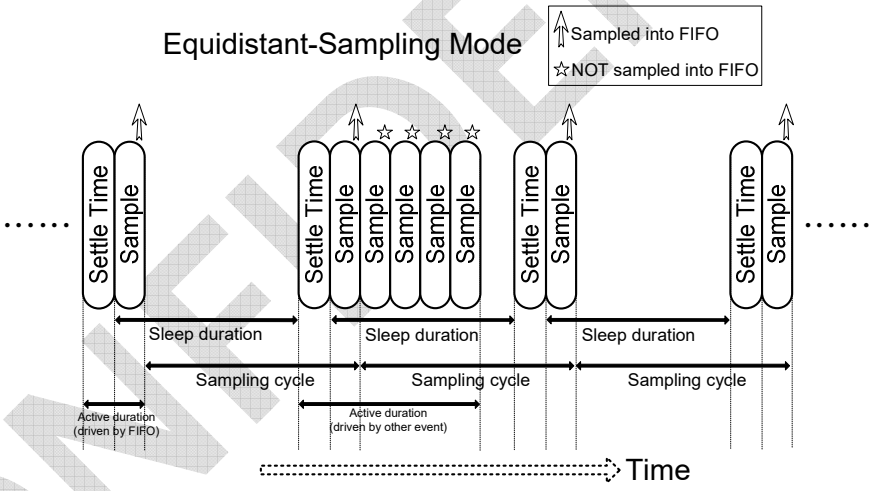
In **Suspend Mode**, whole analog and oscillator are power-down. No data acquisition is performed. Only register reading and writing to SUSPEND bit in register POWMODE (0x11) or register SWRST (0x14) are supported. Suspend mode can be entered by set SUSPEND bit in register POWMODE (0x11) to 1. In the suspend mode, the output data doesn't clear or update, but keeps the last value before entering suspend mode.

In **Low-Power Mode**, STK8321-W will switch between wake-up and sleep phase. In wake-up phase, the device is full functional operation, just like in Normal Mode. In sleep phase, the analog circuit is power-down except oscillator. Average current consumption can be effectively reduced by entering low-power mode. Low-power mode can be entered by setting LOWPOWER bit in register POWMODE (0x11) to 1.

Two kinds timing behaviors of low-power mode, event-driven mode (EDM) and equidistant-sampling mode (ESM), it can be selected by SLEEP_TIMER bit in register POWMODE (0x11). When SLEEP_TIMER is set to '0', the event-driven mode (EDM) is selected. In EDM, the duration of the wake-up phase depends on the number of samples required by the enabled interrupt engines. If an interrupt is detected, the device stays in the wake-up phase as long as the interrupt condition endures (non-latched interrupt), or until the latch time expires (temporary interrupt), or until the interrupt is reset (latched interrupt). If no interrupt is detected, the device enters the sleep phase immediately after the required number of acceleration samples have been taken and an active interface access cycle has ended. The EDM mode is recommended for power-critical applications which do not use the FIFO. The figure below shows the timing diagram for low-power modes when EDM is selected.



When SLEEP_TIMER is set to '1', the equidistant-sampling mode (ESM) is selected. The ESM is recommended when the FIFO is used since it ensures that equidistant samples are sampled into the FIFO regardless of whether the active phase is extended by active interrupt engines or interface activity. In ESM, the sleep duration is defined as shown in following figure. The FIFO sampling cycle is the sum of the sleep duration and the sensor settling time. Since interrupt engines can extend the active phase to exceed the sleep duration, equidistant sampling is only guaranteed if the bandwidth has been chosen such that 1/(2 * bandwidth) = n * (sleep duration) where n is an integer. If this condition is infringed, equidistant sampling is not possible. Once the sleep time has elapsed the device will store the next available sample in the FIFO. This set-up condition is not recommended as it may result in timing jitter.



The duration of sleep phase can be set by SLEEP_DUR [3:0] in register POWMODE (0x11).

SLEEP_DUR[3:0]	Duration (ms)	Actually ODR with 1kHz bandwidth (Hz)
4'b0000 ~ 4'b0101	0.5	295
4'b0110	1	255
4'b0111	2	202
4'b1000	4	140
4'b1001	6	110
4'b1010	10	75
4'b1011	25	34
4'b1100	50	18
4'b1101	100	10
4'b1110	500	2
4'b1111	1000	1

8.3 Data, Range and Bandwidth

Acceleration Data

The acceleration data of STK8321-W is 12 bits and is given in two's complement format. The MSB in each axis will be stored in register XOUT2/YOUT2/ZOUT2 (0x03, 0x05, 0x07) individually, and the LSB will be stored in register XOUT1/YOUT1/ZOUT1 (0x02, 0x04, 0x06) individually. The NEW_X/NEW_Y/NEW_Z bit in register XOUT1/YOUT1/ZOUT1 (0x02, 0x04, 0x06) is used for new data flag, and it will be set to 1 if the data is updated, and reset if either the corresponding MSB or LSB is read. Reading the acceleration data registers shall always start with the LSB part due to the data protection function. When data protection function is enabled, the content of an MSB register will be updated by reading the corresponding LSB register. The data protection function can be disabled (enabled) by writing '1' (‘0’) to the PROTECT_DIS bit in register DATASETUP (0x13). With disabled data protection, the content of both MSB and LSB registers is updated by a new value immediately.

Range

The STK8321-W supports four different acceleration measurement ranges. A measurement range can be selected by RANGE[3:0] bits in register RANGESEL (0x0F).

RANGE[3:0]		Sensing Range	Resolution
4’b0011	0x3	±2g	0.98 mg/LSB
4’b0101	0x5	±4g	1.95 mg/LSB
4’b1000	0x8	±8g	3.91 mg/LSB
others		undefined	undefined

Bandwidth

There are two different data stream of STK8321-W, unfiltered data and filtered data. Unfiltered data is sampled as 2 kHz, and the sample rate of filtered data depends on the selected bandwidth; it is twice of the bandwidth. If the DATA_SEL bit in register DATASETUP (0x13) is set to '0' ('1'), the filtered (unfiltered) data will be stored in the XOUT/YOUT/ZOUT data register. Each of the data stream can be separately offset-compensated, and also can be the data source of interrupts controller. The actual bandwidth for the filtered data can be selected by BW [4:0] bits in register BWSEL (0x10).

BW[4:0]	Actual Bandwidth (Hz)
5’b00xxx	7.81
5’b01000	7.81
5’b01001	15.63
5’b01010	31.25
5’b01011	62.5
5’b01100	125
5’b01101	250
5’b01110	500
5’b01111	1000
5’b1xxxx	1000

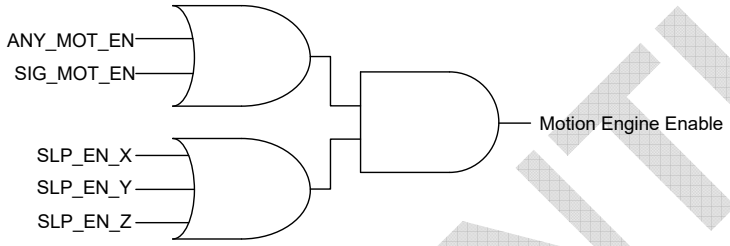
8.4 Motion Algorithm Status and Interrupt Event Detection

The following table shows the interrupt events offered by STK8321-W. Several interrupt engines and two INT pins are integrated for conveniently motion detection. Each interrupt could be enabled independently, and mapped into any of two INT pins. If the condition of enabled interrupt is fulfilled, the corresponding status is set to ‘1’ and selected INT pin is asserted. The INT pin state is logical ‘or’ combination of all mapped interrupts. The INT pin state is logical ‘or’ combination of all mapped interrupts. If an interrupt is disabled, all active pins and status are reset immediately.

Two motion algorithms, any-motion and significant motion, used for detecting user movement can flexibly choose three independent axes as the data source via register INTEN1 (0x16), and the event signal is triggered by an “OR” combination of the enabled axes.

Interrupt Event	Control Bit	Status Bit in Register INTSTS1/2 (0x09, 0x0A)
New Data	DATA_EN in INTEN2 (0x17)	DATA_STS
Any-Motion (Slope) Significant Motion	SLP_EN_Z in INTEN1 (0x16) SLP_EN_Y in INTEN1 (0x16) SLP_EN_X in INTEN1 (0x16)	SLP_1ST_Z SLP_1ST_Y SLP_1ST_X
	ANY_MOT_EN in SIGMOT2 (0x2A)	ANY_MOT_STS
	SIG_MOT_EN in SIGMOT2 (0x2A)	SIG_MOT_STS

Note: Motion algorithm engine follows the logic shown below.



Interrupt Latch Mode

There are three different interrupt latch modes of Any-Motion (Slope) and Significant Motion: non-latched, temporary, and latched. The modes can be selected by the INT_LATCH [3:0] bits in register INTCFG2 (0x21). The following table shows the different configurations of interrupt modes in INT_LATCH [3:0].

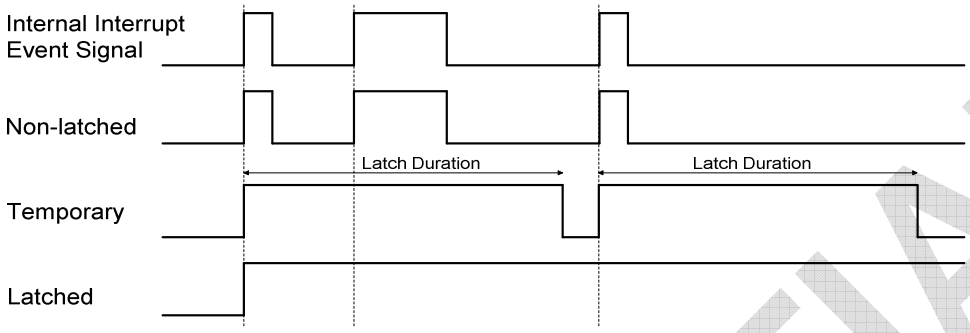
INT_LATCH[3:0]	Output Mode
4’b0000	non-latched
4’b0001	temporary, 250ms
4’b0010	temporary, 500ms
4’b0011	temporary, 1s
4’b0100	temporary, 2s
4’b0101	temporary, 4s
4’b0110	temporary, 8s
4’b0111	latched
4’b1000	non-latched
4’b1001	temporary, 250us
4’b1010	temporary, 500us
4’b1011	temporary, 1ms
4’b1100	temporary, 12.5ms
4’b1101	temporary, 25ms
4’b1110	temporary, 50ms
4’b1111	latched

In the **non-latched mode**, the corresponding status and mapped INT pin are clear as soon as the activation condition is no more valid.

In the **latched mode**, the status and mapped INT pins are cleared only by setting ‘1’ to the INT_RST bit in register INTCFG2 (0x21). If the activation condition still holds when it is cleared, the interrupt pin and status will be both asserted again.

In the **temporary mode**, an asserted interrupt and selected pin are cleared after a defined period of time. The following figure shows the behavior of three interrupt modes.

Both filtered and unfiltered data could be the data source of the interrupt events. Setting the corresponding bit in register DATASETUP (0x13) to ‘0’(‘1’) will select the filtered(unfiltered) data as the data source for interrupt events.



Interrupt latch mode control bits only apply to Any-Motion (Slope) and Significant Motion. Other interrupt events are fixed to their own latch mode which are shown in the following table.

Interrupt Event	Type	Latch mode	Clear
New data	Status	Non-latch	Auto clear after data update
Any-Motion (Slope)	Programmable	Programmable	Based on configuration
Significant Motion	Programmable	Programmable	Based on configuration
FIFO Watermark	Status	Non-latch	After the event is invalid
FIFO Full	Status	Non-latch	After the event is invalid

Interrupt Pin Mapping and Output Types

The mapping of interrupts to the INT1 or INT2 is controlled by registers INTMAP2 (0x1A). Setting the corresponding bit to ‘1’(‘0’) maps(un-maps) the related interrupt to the INT pins.

Both INT1 and INT2 can be configured in register INTCFG1 (0x20). The output and active level can be set as Push-Pull/Open-Drain and as active-high/active-low.

8.5 Offset Compensation

Manual Compensation

STK8321-W offers the manual digital offset-compensation method. It is done by adding a compensation value to the acceleration data coming from the ADC. The registers OFSTX/Y/Z (0x38, 0x39, 0x3A) are used to for the offset compensation purpose and are given in two's complement format. 1 LSB of OFSTX/Y/Z represents 7.81mg in any sensing range. By writing '1' to the OFST_RST bit in register OFSTCOMP1 (0x36), all offset compensation registers are reset to zero.

It is recommended to write into these registers immediately after a new data interrupt in order not to disturb running offset computations.

8.6 FIFO

FIFO Operating Modes

The STK8321-W features an integrated FIFO memory capable of storing up to 32 frames, which allows collecting 32 samples of 12 bits for the x, y and z- axis data at the same point on the timeline or storing 96 samples of 12 bits for the single axis data.

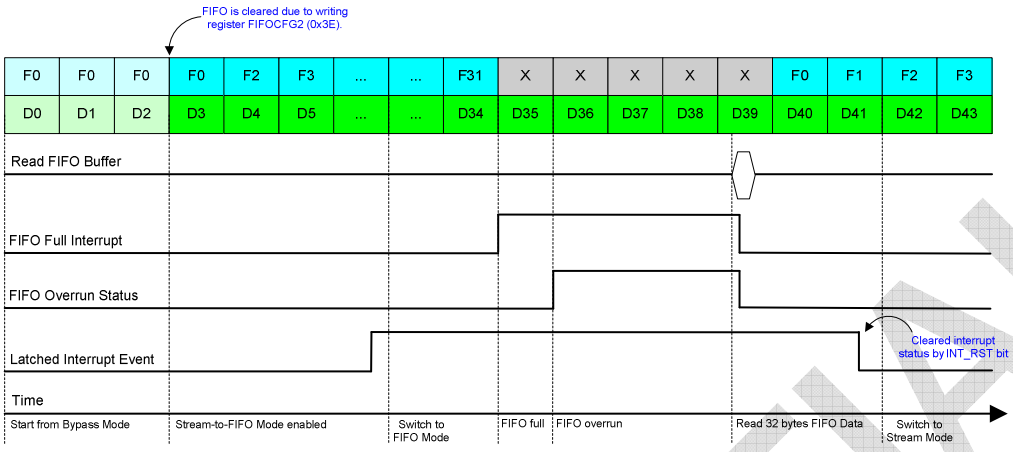
FIFO use allows consistent power saving for the system, it can wake up only when needed and burst the data out from the FIFO. The FIFO buffer can work according to five different modes: Bypass mode, FIFO mode, Stream mode, Bypass-to-Stream and Stream-to-FIFO mode.

In **Bypass mode**, only the current sensor data can be read out from the FIFO address. Essentially, the FIFO behaves like the Stream mode with a depth of 1. If user reads the acceleration data from FIFO data register, it can be guaranteed that the x, y, and z- axis data are from the same timestamp. To avoid mixing of data from different axes occur while the data registers are updated sequentially. When new data arrives, the old data will be overwritten and the overrun bit is set to '1'.

In **FIFO mode**, the acceleration data of the selected axes are continuously stored in the buffer until the unread data reaches 32 frames for x, y, z- axis or 96 frames for the single axis. When the FIFO is full, the data collection is stopped and new data is ignored. If FIFO mode is enabled, a watermark interrupt will be triggered when the buffer is filled to a configurable level. Once the buffer is full, a FIFO-full interrupt also generates if it has been enabled.

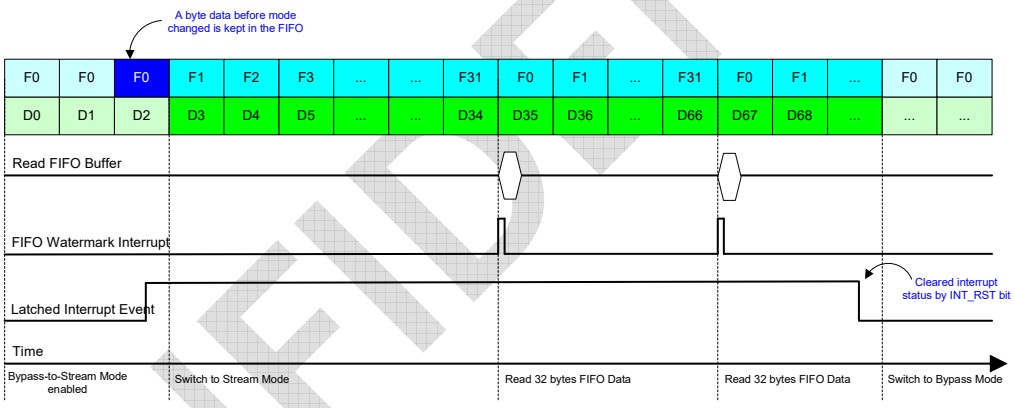
In **Stream mode**, the acceleration data of the selected axes are continuously updated in the buffer. When the buffer is full, as new data arrives the oldest data is discarded and overwritten by the newer. If an overrun occurs, the FIFO overrun flag is asserted. If Stream mode enabled, a watermark interrupt is triggered when the buffer is filled to a configurable level. Once the buffer is full, a FIFO-full interrupt generates if it has been enabled.

In **Stream-to-FIFO mode**, the FIFO buffer starts operating in Stream mode and switches to FIFO mode when the Any-Motion (slope) or Significant Motion interrupt occurs. User must be sure that the interrupt is configured to latched mode. When the FIFO is full, data collecting is stopped. This mode can be used for analyzing the samples history which recorded before the interrupt event. The recommendation operation is to read FIFO content after FIFO mode is triggered and FIFO buffer is full and stopped capturing data.



Stream-to-FIFO Mode

In **Bypass-to-Stream mode**, the FIFO buffer starts in Bypass mode and switches to Stream mode when the Any-Motion (slope) or Significant Motion interrupt occurs. User must be sure that interrupt is configured to the latched mode. This mode can be used for analyzing the samples after event occurred. In this mode, user is recommended to enable watermark interrupt to avoid loss of data.



Bypass-to-Stream Mode

Note: When the requested event takes place, the FIFO mode change is triggered if and only if the event flag is routed to the INT1 in Stream-to-FIFO mode and Bypass-to-Stream mode.

The FIFO operation can be controlled by register FIFOCFG2 (0x3E) FIFO_MODE[2:0], and the corresponding settings are shown in the table below.

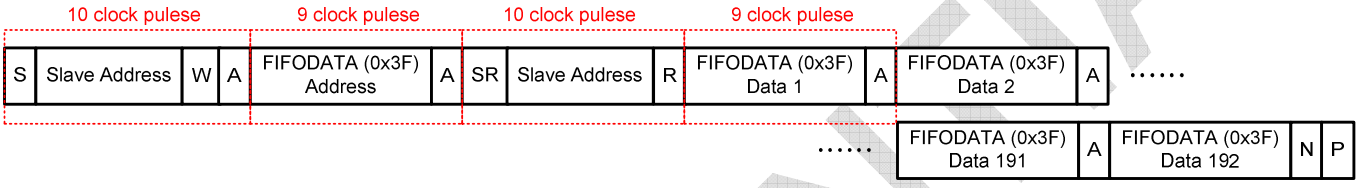
FIFO_MODE[2:0]	Mode selection
3'b000	Bypass mode
3'b001	FIFO mode
3'b010	reserved
3'b011	Stream-to-FIFO mode
3'b100	Bypass-to-Stream mode
3'b101	reserved
3'b110	Stream mode
3'b111	reserved

The FIFO content, full interrupt, and watermark interrupt will be cleared and reset when writing to register FIFOCFG1 (0x3D) or register FIFOCFG2 (0x3E).

FIFO Data Readout

The latest frame stored in FIFO is identical to the acceleration data in the read-out registers (0x02) to (0x07). Thus, all configuration settings apply to the FIFO frame as well as the acceleration data readout registers. The readout can be performed using burst mode since the read address counter is no longer incremented, when the burst read access starts below address FIFODATA (0x3F). A single burst is recommended to read out one or more frames at a time.

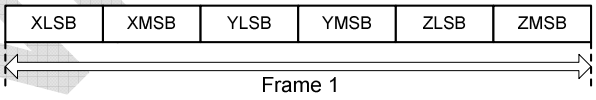
The I2C needs about 29 clock pulses to start communication plus an additional 9 clock pulses for every byte to read. So, in the case of I2C standard mode being used (100 kHz), total 32 frames XYZ-axes FIFO data reading takes (29 + 9 * 32 * 6) clock pulses, about 17.57 ms. In another case of I2C fast mode being used (400 kHz), it takes about 4.39 ms.



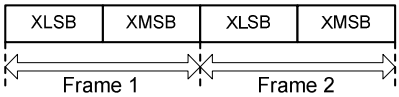
Register FIFOCFG2 (0x3E) FIFO_DATA_SEL[1:0] controls the acceleration data of which axes are stored in the FIFO. The depth of the FIFO depends on whether all or a single axis is selected. Moreover, FIFO_INTERVAL[1:0] controls the acceleration data storage interval, and users can select the subsampling frequency in every one, two, four, or eight samples that the acceleration data will be automatically stored into FIFO. The buffer content, FIFO full interrupt and watermark interrupt are cleared and reset if user write to the register FIFOCFG1 (0x3D) or FIFOCFG2 (0x3E).

FIFO_DATA_SEL [1:0]	FIFO data source
2'b00	XYZ-axes
2'b01	X-axis only
2'b10	Y-axis only
2'b11	Z-axis only

If all axes are enabled, the format of the data read-out from register FIFODATA (0x3F) is as follows:



If only one axis is enabled, the format of the data read-out from register FIFODATA (0x3F) is as follows:
(Example shown x-axis only, other axes are equivalent).



To be sure the data integrity, a frame shall be the minimum unit for FIFO reading. If a frame is not properly read due to an incomplete read operation, the remaining part of the frame is discarded.

If user read out a length of frame data which is beyond the FIFO fill level, zeroes (0, 0, 0) will be presented.

FIFO Frame Counter and Overrun Flag

Register FIFOSTS (0x0C) FIFO_FRAME_CNT[6:0] indicates the current frame level of the buffer. The FIFO_OVR bit will be set as '1' if a new frame arrives but the FIFO is full. Once the frames are read out and FIFO_FRAME_CNT[6:0] is decremented, the FIFO_OVR bit will be reset to '0'.

The FIFO buffer, FIFO_FRAME_CNT[6:0], and FIFO_OVR bit are all reset when user writes to FIFOCFG1 (0x3D) or FIFOCFG2 (0x3E).

FIFO Interrupts

The FIFO controller can generate two different interrupt events, a FIFO-full and a watermark event. The FIFO-full and watermark interrupts are both available in all FIFO operating modes.

In order to enable the watermark interrupt, the register INTEN2 (0x17) FWM_EN bit and register INTMAP2 (0x1A) FWM2INT1 or FWM2INT2 bit must be set to '1' that routes the interrupt signal to INT1 or INT2 pins.

The watermark interrupt is asserted when the frames level in the buffer reaches the level defined by register FIFOCFG1 (0x3D) FIFO_WM_LV. Meanwhile, the status of the watermark interrupt can be read back via register INTSTS2 (0x0A) FWM_STS bit.

In order to enable the FIFO-full interrupt, register INTEN2 (0x17) FFULL_EN bit as well as register INTMAP2 (0x1A) FFULL2INT1 or FFULL2INT2 bit must also be set to '1'. The FIFO-full interrupt is triggered when the buffer has been fully occupied and that means 32 frames in FIFO mode, 32 frames in Stream mode, and 1 frame in Bypass mode. The status of the FIFO-full interrupt is also shown in register INTSTS2 (0x0A) FFULL_STS bit.

The interrupts and status of FIFO-full and watermark will both be reset after writing to register FIFOCFG1 (0x3D) or FIFOCFG2 (0x3E) and the FIFO buffer is also simultaneously cleared.

9. REGISTER DEFINATION

9.1 Register Map

ADDR	REG NAME	BIT 7	6	5	4	3	2	1	0	Default
00h	CHIP_ID	CHIP_ID[7:0]								23h
01h	RESERVED	reserved								00h
02h	XOUT1	XOUT[3:0]				reserved				00h
03h	XOUT2	XOUT[11:4]								00h
04h	YOUT1	YOUT[3:0]				reserved				00h
05h	YOUT2	YOUT[11:4]								00h
06h	ZOUT1	ZOUT[3:0]				reserved				00h
07h	ZOUT2	ZOUT[11:4]								00h
08h	RESERVED	reserved								00h
09h	INTSTS1	reserved					ANY_MOT_STS	reserved	SIG_MOT_STS	00h
0Ah	INTSTS2	DATA_STS	FWM_STS	FFULL_STS	reserved					00h
0Bh	EVENTINFO1	reserved	SLPSIGN_Z	SLPSIGN_Y	SLPSIGN_X	reserved	SLP_1ST_Z	SLP_1ST_Y	SLP_1ST_X	00h
0Ch	FIFOSTS	FIFO_OVR	FIFO_FRAME_CNT[6:0]							00h
0D-0Eh	RESERVED	reserved								00h
0Fh	RANGESEL	reserved				RANGE[3:0]				03h
10h	BWSEL	reserved			BW[4:0]					1Fh
11h	POWMODE	SUSPEND	LOWPOWER	SLEEP_TIMER	SLEEP_DUR[3:0]				reserved	00h
12h	RESERVED	reserved								00h
13h	DATASETUP	DATA_SEL	PROTECT_DIS	reserved						00h
14h	SWRST	SWRST[7:0]								00h
15h	RESERVED	reserved								00h
16h	INTEN1	reserved					SLP_EN_Z	SLP_EN_Y	SLP_EN_X	00h
17h	INTEN2	reserved	FWM_EN	FFULL_EN	DATA_EN	reserved				00h
18h	RESERVED	reserved								00h
19h	INTMAP1	SIGMOT2INT2	reserved	ANYMOT2INT2	reserved		ANYMOT2INT1	reserved	SIGMOT2INT1	00h
1Ah	INTMAP2	DATA2INT2	FWM2INT2	FFULL2INT2	reserved		FFULL2INT1	FWM2INT1	DATA2INT1	00h
1Bh-1Fh	RESERVED	reserved								00h
20h	INTCFG1	reserved				INT2_OD	INT2_LV	INT1_OD	INT1_LV	05h
21h	INTCFG2	INT_RST	reserved			INT_LATCH[3:0]				00h
22h-26h	RESERVED	reserved								00h
27h	SLOPEDLY	reserved						SLP_DUR[1:0]		00h
28h	SLOPETHD	SLP_THD[7:0]								14h
29h	SIGMOT1	SKIP_TIME[7:0]								96h
2Ah	SIGMOT2	reserved					ANY_MOT_EN	SIG_MOT_EN	SKIP_TIME[8]	02h
2Bh	SIGMOT3	reserved	PROOF_TIME[6:0]							32h
2Ch-32h	RESERVED	reserved								00h
33h	PRIMIF	SPI_PRIMARY[7:0]								00h
34h	INTFCFG	reserved					I2C_WDT_EN	I2C_WDT_SEL	SPI_3WM	00h
35h	RESERVED	reserved								00h

36h	OFSTCOMP1	OFST_RST	reserved					**00h**
37h	RESERVED	reserved						**00h**
38h	OFSTX	OFST_X[7:0]						**00h**
39h	OFSTY	OFST_Y[7:0]						**00h**
3Ah	OFSTZ	OFST_Z[7:0]						**00h**
3Bh-3Ch	RESERVED	reserved						**00h**
3Dh	FIFOCFG1	reserved	FIFO_WM_LV[6:0]					**00h**
3Eh	FIFOCFG2	FIFO_MODE[2:0]		reserved	FIFO_INTERVAL[1:0]		FIFO_DATA_SEL[1:0]	**00h**
3Fh	FIFODATA	FIFOOUT[7:0]						**00h**

9.2 Register Description

CHIP_ID Register (00h)

b7	b6	b5	b4	b3	b2	b1	b0
CHIP_ID[7:0]							
8'b00100011							
RO							

The register contains the chip identification code.

XOUT1 Register (02h)

b7	b6	b5	b4	b3	b2	b1	b0
XOUT[3:0]				reserved			
4'b0000				4'b0000			
RO				RO			

XOUT1/XOUT2 register contain the x-axis acceleration data.

XOUT2 Register (03h)

b7	b6	b5	b4	b3	b2	b1	b0
XOUT[11:4]							
8'b00000000							
RO							

YOUT1 Register (04h)

b7	b6	b5	b4	b3	b2	b1	b0
YOUT[3:0]				reserved			
4'b0000				4'b0000			
RO				RO			

YOUT1/YOUT2 register contain the y-axis acceleration data.

YOUT2 Register (05h)

b7	b6	b5	b4	b3	b2	b1	b0
YOUT[11:4]							
8'b00000000							
RO							

ZOUT1 Register (06h)

b7	b6	b5	b4	b3	b2	b1	b0
ZOUT[3:0]				reserved			
4'b0000				4'b0000			
RO				RO			

ZOUT1/ZOUT2 register contain the z-axis acceleration data.

ZOUT2 Register (07h)

b7	b6	b5	b4	b3	b2	b1	b0
ZOUT[11:4]							
8'b00000000							
RO							

INTSTS1 Register (09h)

b7	b6	b5	b4	b3	b2	b1	b0
reserved					ANY_MOT_STS	reserved	SIG_MOT_STS
5'b00000					0	0	0
RO					RO	RO	RO

This register contains the interrupts status in STK8321-W.

BIT	BIT NAME	Description
0	SIG_MOT_STS	Significant motion interrupt status. '1' : event triggered, '0' : no event.
2	ANY_MOT_STS	Any-motion (slope) detection interrupt status. '1' : event triggered, '0' : no event.

INTSTS2 Register (0Ah)

b7	b6	b5	b4	b3	b2	b1	b0
DATA_STS	FWM_STS	FFULL_STS	reserved				
0	0	0	5'b00000				
RO	RO	RO	RO				

This register contains the new data interrupt status in STK8321-W.

BIT	BIT NAME	Description
5	FFULL_STS	FIFO full interrupt status. '1' : event triggered, '0' : no event.
6	FWM_STS	FIFO watermark interrupt status. '1' : event triggered, '0' : no event.
7	DATA_STS	New data interrupt status. '1' : event triggered, '0' : no event.

EVENTINFO1 Register (0Bh)

b7	b6	b5	b4	b3	b2	b1	b0
reserved	SLPSIGN_Z	SLPSIGN_Y	SLPSIGN_X	reserved	SLP_1ST_Z	SLP_1ST_Y	SLP_1ST_X
0	0	0	0	0	0	0	0
RO	RO	RO	RO	RO	RO	RO	RO

This register contains any-motion (slope) detection information.

BIT	BIT NAME	Description
0	SLP_1ST_X	1 : Motion on the X-axis cause SLOPE interrupt asserted.
1	SLP_1ST_Y	1 : Motion on the Y-axis cause SLOPE interrupt asserted.
2	SLP_1ST_Z	1 : Motion on the Z-axis cause SLOPE interrupt asserted.
4	SLPSIGN_X	Sign of acceleration slope on the X-axis that triggered the SLOPE interrupt. 0 : positive. 1 : negative.
5	SLPSIGN_Y	Sign of acceleration slope on the Y-axis that triggered the SLOPE interrupt. 0 : positive. 1 : negative.
6	SLPSIGN_Z	Sign of acceleration slope on the Z-axis that triggered the SLOPE interrupt. 0 : positive. 1 : negative.

FIFOSTS Register (0Ch)

b7	b6	b5	b4	b3	b2	b1	b0
FIFO_OVR	FIFO_FRAME_CNT[6:0]						
0	7'b00000000						
RO	RO						

This register contains FIFO status flags.

BIT	BIT NAME	Description
7	FIFO_OVR	FIFO overrun flag. '1' : event triggered, '0' : no event. Flag can be cleared by reading data from FIFODATA[7:0].
[6:0]	FIFO_FRAME_CNT[6:0]	Current fill level of FIFO buffer, it shows the number of unread frames stored in FIFO.

RANGESEL Register (0Fh)

b7	b6	b5	b4	b3	b2	b1	b0
reserved				RANGE[3:0]			
4'b0000				4'b0011			
RO				R/W			

This register contains the acceleration sensing range. It is recommended that set the suspend mode before changing the register RANGESEL(0x0F) to ensure correct output data.

RANGE[3:0]		Sensing Range
4'b0011	0x3	±2g
4'b0101	0x5	±4g
4'b1000	0x8	±8g
others		undefined

BWSEL Register (10h)

b7	b6	b5	b4	b3	b2	b1	b0
reserved			BW[4:0]				
3'b000			5'b11111				
RO			R/W				

This register contains the output data bandwidth selection. It is recommended that set the suspend mode before changing the register BWSEL(0x10) to ensure correct output data.

BW[4:0]	Actual Bandwidth (Hz)
5'b00xxx	7.81
5'b01000	7.81
5'b01001	15.63
5'b01010	31.25
5'b01011	62.5
5'b01100	125
5'b01101	250
5'b01110	500
5'b01111	1000
5'b1xxxx	1000

POWMODE Register (11h)

b7	b6	b5	b4	b3	b2	b1	b0
SUSPEND	LOWPOWER	SLEEP_TIMER	SLEEP_DUR[3:0]				reserved
0	0	0	4'b0000				0
R/W	R/W	R/W	R/W				RO

This register contains the power mode selection and the sleep time duration setting. It is recommended that set the suspend mode before changing the register POWMODE(0x11) to ensure correct output data.

<table>
<tr><th>BIT</th><th>BIT NAME</th><th>Description</th></tr>
<tr><td>[4:1]</td><td>SLEEP_DUR[3:0]</td><td>Sleep time duration.
<table>
<tr><td>SLEEP_DUR[3:0]</td><td>Duration (ms)</td></tr>
<tr><td>4’b0000 ~ 4’b0101</td><td>0.5</td></tr>
<tr><td>4’b0110</td><td>1</td></tr>
<tr><td>4’b0111</td><td>2</td></tr>
<tr><td>4’b1000</td><td>4</td></tr>
<tr><td>4’b1001</td><td>6</td></tr>
<tr><td>4’b1010</td><td>10</td></tr>
<tr><td>4’b1011</td><td>25</td></tr>
<tr><td>4’b1100</td><td>50</td></tr>
<tr><td>4’b1101</td><td>100</td></tr>
<tr><td>4’b1110</td><td>500</td></tr>
<tr><td>4’b1111</td><td>1000</td></tr>
</table></td></tr>
<tr><td>5</td><td>SLEEP_TIMER</td><td>Sleep timer control bit in low-power mode.
0 : event-driven.
1 : equidistant sampling.</td></tr>
<tr><td>6</td><td>LOWPOWER</td><td>0 : low-power mode disable.
1 : low-power mode enable.</td></tr>
<tr><td>7</td><td>SUSPEND</td><td>0 : suspend mode disable.
1 : suspend mode enable.</td></tr>
</table>

DATASETUP Register (13h)

b7	b6	b5	b4	b3	b2	b1	b0
DATA_SEL	PROTECT_DIS	reserved					
0	0	6’b000000					
R/W	R/W	RO					

This register is used to select if the output data is filtered or unfiltered and how the output data contained in the register XOUT1/XOUT2, YOUT1/YOUT2, ZOUT1/ZOUT2 are updated.

BIT	BIT NAME	Description
6	PROTECT_DIS	0 : Enable the data protection function. 1 : Disable the data protection function.
7	DATA_SEL	0 : Data output filtered. 1 : Data output unfiltered.

SWRST Register (14h)

b7	b6	b5	b4	b3	b2	b1	b0
SWRST[7:0]							
8’b00000000							
W							

This register is used to software reset. Write 0xB6 into SWRST to reset all the registers to default value.

INTEN1 Register (16h)

b7	b6	b5	b4	b3	b2	b1	b0
reserved					SLP_EN_Z	SLP_EN_Y	SLP_EN_X
5’b00000					0	0	0
RO					R/W	R/W	R/W

This register contains the several interrupt enable bit.

BIT	BIT NAME	Description
0	SLP_EN_X	0 : Disable X-axis any-motion (slope) interrupt. 1 : Enable X-axis any-motion (slope) interrupt.
1	SLP_EN_Y	0 : Disable Y-axis any-motion (slope) interrupt. 1 : Enable Y-axis any-motion (slope) interrupt.
2	SLP_EN_Z	0 : Disable Z-axis any-motion (slope) interrupt. 1 : Enable Z-axis any-motion (slope) interrupt.

INTEN2 Register (17h)

b7	b6	b5	b4	b3	b2	b1	b0
reserved	FWM_EN	FFULL_EN	DATA_EN	reserved			
0	0	0	0	4'b0000			
RO	R/W	R/W	R/W	RO			

This register contains the several interrupt enable bit.

BIT	BIT NAME	Description
4	DATA_EN	0 : Disable new data interrupt. 1 : Enable new data interrupt.
5	FFULL_EN	0 : Disable FIFO full interrupt. 1 : Enable FIFO full interrupt.
6	FWM_EN	0 : Disable FIFO watermark interrupt. 1 : Enable FIFO watermark interrupt.

INTMAP1 Register (19h)

b7	b6	b5	b4	b3	b2	b1	b0
SIGMOT2INT2	reserved	ANYMOT2INT2	reserved		ANYMOT2INT1	reserved	SIGMOT2INT1
0	0	0	2'b00		0	0	0
R/W	RO	R/W	RO		R/W	RO	R/W

This register is used to map the related interrupt to the desired INT pin.

BIT	BIT NAME	Description
0	SIGMOT2INT1	0 : Do not map significant motion interrupt to INT1. 1 : Map significant motion interrupt to INT1.
2	ANYMOT2INT1	0 : Do not map any-motion (slope) interrupt to INT1. 1 : Map any-motion (slope) interrupt to INT1.
5	ANYMOT2INT2	0 : Do not map any-motion (slope) interrupt to INT2. 1 : Map any-motion (slope) interrupt to INT2.
7	SIGMOT2INT2	0 : Do not map significant motion interrupt to INT2. 1 : Map significant motion interrupt to INT2.

INTMAP2 Register (1Ah)

b7	b6	b5	b4	b3	b2	b1	b0
DATA2INT2	FWM2INT2	FFULL2INT2	reserved		FFULL2INT1	FWM2INT1	DATA2INT1
0	0	0	2'b00		0	0	0
R/W	R/W	R/W	RO		R/W	R/W	R/W

This register is used to map the related interrupt to the desired INT pin.

BIT	BIT NAME	Description
0	DATA2INT1	0 : Do not map new data interrupt to INT1. 1 : Map new data interrupt to INT1.
1	FWM2INT1	0 : Do not map FIFO watermark interrupt to INT1. 1 : Map FIFO watermark interrupt to INT1.
2	FFULL2INT1	0 : Do not map FIFO full interrupt to INT1. 1 : Map FIFO full interrupt to INT1.
5	FFULL2INT2	0 : Do not map new data interrupt to INT2. 1 : Map new data interrupt to INT2.
6	FWM2INT2	0 : Do not map FIFO watermark interrupt to INT2. 1 : Map FIFO watermark interrupt to INT2.
7	DATA2INT2	0 : Do not map FIFO full interrupt to INT2. 1 : Map FIFO full interrupt to INT2.

INTCFG1 Register (20h)

b7	b6	b5	b4	b3	b2	b1	b0
reserved				INT2_OD	INT2_LV	INT1_OD	INT1_LV
4'b0000				0	1	0	1
RO				R/W	R/W	R/W	R/W

This register is used to define the INT1 and INT2 pins output type and active level. Open-drain or Push-pull output type and active high or active low can be selected.

BIT	BIT NAME	Description
0	INT1_LV	INT1 active level selection. 0 : Active low. 1 : Active high.
1	INT1_OD	INT1 output type selection. 0 : Push-pull output type. 1 : Open-drain output type.
2	INT2_LV	INT2 active level selection. 0 : Active low. 1 : Active high.
3	INT2_OD	INT2 output type selection. 0 : Push-pull output type. 1 : Open-drain output type.

INTCFG2 Register (21h)

b7	b6	b5	b4	b3	b2	b1	b0
INT_RST	reserved			INT_LATCH[3:0]			
0	3'b000			4'b0000			
R/W	RO			R/W			

This register is used to reset latched interrupt pin and select the interrupt mode.

BIT	BIT NAME	Description
[3:0]	INT_LATCH[3:0]	INT pin output mode selection. INT_LATCH[3:0] / Output Mode 4'b0000 non-latched 4'b0001 temporary, 250ms 4'b0010 temporary, 500ms 4'b0011 temporary, 1s 4'b0100 temporary, 2s 4'b0101 temporary, 4s 4'b0110 temporary, 8s 4'b0111 latched 4'b1000 non-latched 4'b1001 temporary, 250us 4'b1010 temporary, 500us 4'b1011 temporary, 1ms 4'b1100 temporary, 12.5ms 4'b1101 temporary, 25ms 4'b1110 temporary, 50ms 4'b1111 latched
7	INT_RST	1 : Reset any latched interrupt pin.

SLOPEDLY Register (27h)

b7	b6	b5	b4	b3	b2	b1	b0
reserved						SLP_DUR[1:0]	
6'b000000						2'b00	
RO						R/W	

This register is used to set the number of samples needed in slope detection. The actual number of samples will be equal to SLP_DUR[1:0] + 1.

SLOPETHD Register (28h)

b7	b6	b5	b4	b3	b2	b1	b0
SLP_THD[7:0]							
8'b00010100							
R/W							

This register is used to set the threshold value for the slope detection. The actual slope threshold will depend on sensing range. The default value of SLP_THD[7:0] is 0x14.

RANGE[3:0]	Sensing Range	Actual Slope Threshold (mg)
4'b0011	±2g	SLP_THD[7:0] * 3.91
4'b0101	±4g	SLP_THD[7:0] * 7.81
4'b1000	±8g	SLP_THD[7:0] * 15.63

SIGMOT1 Register (29h)

b7	b6	b5	b4	b3	b2	b1	b0
SKIP_TIME[7:0]							
8'b10010110							
R/W							

This register is used to set the skip time for the significant motion. Holding the duration for skip, for which the motion is checked for re-detection. 1 LSB=20 ms. Range is 0 to 10sec. The default value of SKIP_TIME[8:0] is 0x96 correspond to 3 seconds.

SIGMOT2 Register (2Ah)

b7	b6	b5	b4	b3	b2	b1	b0
reserved					ANY_MOT_EN	SIG_MOT_EN	SKIP_TIME[8]
5'b00000					0	1	0
RO					R/W	R/W	R/W

This register contains MSB of SKIP_TIME[8:0] for the significant motion, and significant motion interrupt enable bit.

BIT	BIT NAME	Description
1	SIG_MOT_EN	0 : Disable significant motion. 1 : Enable significant motion.
2	ANY_MOT_EN	0 : Disable any-motion. 1 : Enable any-motion.

SIGMOT3 Register (2Bh)

b7	b6	b5	b4	b3	b2	b1	b0
reserved	PROOF_TIME[6:0]						
0	7'b0110010						
RO	R/W						

This register is used to set the proof time for the significant motion. Holding the duration for proof, for which the motion is re-checked after. 1 LSB=20 ms. Range is 0 to 2.5sec. The default value of PROOF_TIME[7:0] is 0x32 correspond to 1 seconds.

PRIMIF Register (33h)

b7	b6	b5	b4	b3	b2	b1	b0
SPI_PRIMARY[7:0]							
8'b00000000							
R/W							

This register is used to set primary communication interface. Write 0x5A into SPI_PRIMARY to set SPI for primary interface.

INTFCFG Register (34h)

b7	b6	b5	b4	b3	b2	b1	b0
reserved					I2C_WDT_EN	I2C_WDT_SEL	SPI_3WM
5'b00000					0	0	0
RO					R/W	R/W	RO

This register contains the digital interface parameters for the I²C or SPI interface.

BIT	BIT NAME	Description
0	SPI_3WM	SPI 3-wire interface activation. 0 : 4-wire SPI interface used. 1 : 3-wire SPI interface used.
1	I2C_WDT_SEL	I²C watchdog timer period selection. 0 : Watchdog timer period 1ms. 1 : Watchdog timer period 50ms.
2	I2C_WDT_EN	I²C watchdog timer enable bit. 0 : Disable I2C watchdog timer. 1 : Enable I2C watchdog timer.

OFSTCOMP1 Register (36h)

b7	b6	b5	b4	b3	b2	b1	b0
OFST_RST	reserved						
0	7'b0000000						
W	RO						

This register is used to define the setting for the offset compensation.

BIT	BIT NAME	Description
7	OFST_RST	1 : Reset all the offset compensation register (register 0x38 ~ 0x3A) to zero.

OFSTX Register (38h)

B7	b6	b5	b4	b3	b2	b1	b0
OFST_X[7:0]							
8'b00000000							
R/W							

This register contains the offset compensation value for the x-axis data output.

OFSTY Register (39h)

B7	b6	b5	b4	b3	b2	b1	b0
OFST_Y[7:0]							
8'b00000000							
R/W							

This register contains the offset compensation value for the y-axis data output.

OFSTZ Register (3Ah)

b7	b6	b5	b4	b3	b2	b1	b0
OFST_Z[7:0]							
8'b00000000							
R/W							

This register contains the offset compensation value for the z-axis data output.

Register 0x38 to 0x3A can be modified manually set by user. The value in these register will be added to the actual acceleration data sensing by STK8321-W and store the new value to XOUT/YOUT/ZOUT register.

FIFOCFG1 Register (3Dh)

b7	b6	b5	b4	b3	b2	b1	b0
reserved	FIFO_WM_LV[6:0]						
0	7'b0000000						
RO	R/W						

This register contains FIFO watermark level. If the number of unread frames in the FIFO is equal to FIFO watermark level, an interrupt will be triggered. Please note writing to register FIFOCFG1 clears the FIFO buffer and overrun flag, and resets FIFO-full and watermark interrupts. If 0, the FIFO watermark interrupt is disabled.

FIFOCFG2 Register (3Eh)

b7	b6	b5	b4	b3	b2	b1	b0
FIFO_MODE[2:0]			reserved	FIFO_INTERVAL[1:0]		FIFO_DATA_SEL[1:0]	
3'b000			0	2'b00		2'b00	
R/W			RO	R/W		R/W	

This register contains FIFO configuration settings. Please note writing to register FIFOCFG2 clears the FIFO buffer and overrun flag, and resets FIFO-full and watermark interrupts.

FIFO_MODE[2:0]	Mode selection
3'b000	Bypass mode
3'b001	FIFO mode
3'b010	reserved
3'b011	Stream-to-FIFO mode
3'b100	Bypass-to-Stream mode
3'b101	reserved
3'b110	Stream mode
3'b111	reserved

FIFO_INTERVAL[1:0]	FIFO data subsampling interval
2'b00	1
2'b01	2
2'b10	4
2'b11	8

FIFO_DATA_SEL [1:0]	FIFO data source
2'b00	XYZ-axes
2'b01	X-axis only
2'b10	Y-axis only
2'b11	Z-axis only

FIFODATA Register (3Fh)

b7	b6	b5	b4	b3	b2	b1	b0
FIFOOUT[7:0]							
8'b00000000							
RO							

This register contains FIFO data output. The format of the LSB and MSB components corresponds to that of the acceleration data readout registers (0x02-0x07). The new data flag is preserved. Read burst access may be used since the address counter will not increment when the read burst is started at the address of FIFODATA. The entire frame is discarded when a frame is only partially read out.

Data format depends on the setting of FIFO_DATA_SEL[1:0], if X+Y+Z data are selected, the data of frame n is reading out in the order of XLSB(n), XMSB(n), YLSB (n), YMSB (n), ZLSB (n), ZMSB (n); if X-only is selected, the data of frame n and n+1 are reading out in the order of XLSB (n), XMSB (n), XLSB (n+1), XMSB(n+1); the Y-only and Z-only modes behave analogously.

10. APPLICATION INFORMATION

10.1 New Data Interrupt

This interrupt serves for synchronous reading of acceleration data. It is generated after storing a new value of z-axis acceleration data in the data register. The interrupt is cleared automatically when the next cycle of data acquisition starts. The interrupt status is '0' for at least 50μs. The interrupt mode of the new data interrupt is keep to non-latched for at least 250 us to 3ms.

Control Register	Bit Name	Function
INTEN2[4]	DATA_EN	'1': enabled, '0': disabled, and the interrupt mode is fixed to non-latched.
INTSTS[7]	DATA_STS	The interrupt status
INTMAP2	DATA2INT1 DATA2INT2	New data interrupt maps to INT1 or INT2.
DATASETUP[5]	DATA_SEL	'1': unfiltered data, '0': filtered data, as the input of the new data interrupt

10.2 Any-motion (Slope) Detection

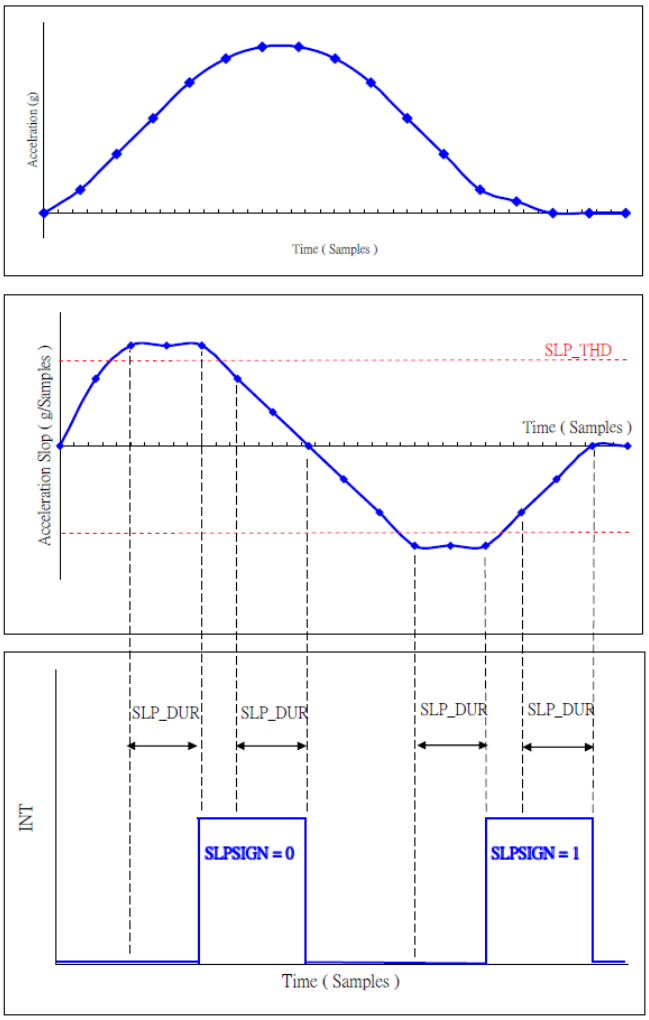
Any-motion (slope) detection is to detect the change of motion. By monitoring the slop of acceleration, user can estimate the variation of acceleration. STK8321-W use the slop between successive acceleration data to detect it, and would active the interrupt when the slop exceeds a preset threshold. Moreover, a duration setting has to be configured to suppress failure signals. The following figure shows the relationship between acceleration data, acceleration slop, and INT status. If a certain number *N* of consecutive slope data points is larger (smaller) than the slope threshold, the INT would be trigger (clear).

One LSB of SLP_THD [7:0] represents 1 LSB of acceleration data, and it depends on which sensing range is set. For Example, 3.91mg in 2g-range, 7.81 mg in 4g-range, 15.6 mg in 8g-range and 31.25 mg in 16g-range. The consecutive slope data points are set by SLP_DUR [1:0], and is equal to (SLP_DUR [1:0] + 1). The time difference between the successive acceleration signals depends on the selected bandwidth and equates to 1/(2*bandwidth).

Any-motion (slope) detection can be enabled by writing '1' to ANY_MOT_EN bit in the register SIGMOT2 (0x2A). Furthermore, user must select which axes are enabled independently by writing '1' to the bit SLP_EN_X, SLP_EN_Y, and SLP_EN_Z in the register INTEN1 (0x16).

If slope of any axis fulfills the specified condition, INT pin would be triggered, interrupt status would be updated to ANY_MOT_STS, and the sign of slop would be shown in SLPSIGN_X, SLPSIGN_Y, SLPSIGN_Z. Moreover, SLP_1ST_X, SLP_1ST_Y, and SLP_1ST_Z would indicate which axis is the first axis triggering the interrupt of slop detection.

Control Register	Bit Name	Function
INTEN1 [0] INTEN1 [1] INTEN1 [2]	SLP_EN_X SLP_EN_Y SLP_EN_Z	Slope detection enable for X-axis, '1': enabled, '0': disabled for Y-axis, '1': enabled, '0': disabled for Z-axis, '1': enabled, '0': disabled
SIGMOT2[2]	ANY_MOT_EN	Any-motion enable bit. 0: Disabled. 1: Enabled.
SLOPETHD [7:0]	SLP_THD	Slope threshold, 1LSB=1LSB of XOUT/YOUT/ZOUT
SLOPEDLY [1:0]	SLP_DUR	Slope duration, 1LSB=1/(2*bandwidth)
INTMAP1	ANTMOT2INT1 ANTMOT2INT2	Slope detection interrupt maps to INT1 or INT2
INTSTS1 [2]	ANT_MOT _STS	Slope detection status which is synchronized with INT1 or INT2 activity
DATASETUP [7]	DATA_SEL	'1': unfiltered data, '0': filtered data, as the input of the slop detection
EVENTINFO1 [0] EVENTINFO1 [1] EVENTINFO1 [2]	SLP_1ST_X SLP_1ST_Y SLP_1ST_Z	'1': triggered axis, '0': not triggered
EVENTINFO1 [4] EVENTINFO1 [5] EVENTINFO1 [6]	SLPSIGN_X SLPSIGN_Y SLPSIGN_Z	Sign of slope when interrupt is triggered, '0': Positive, '1': Negative



10.3 Significant Motion

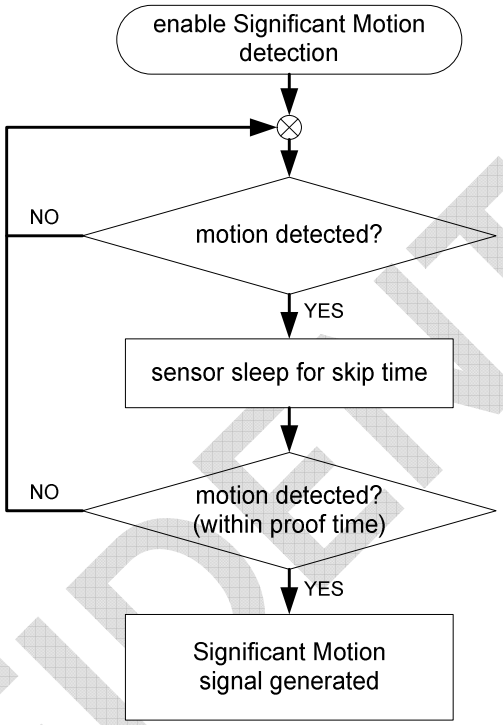
The significant motion is defined as some activities that might lead to a change in a user's location. Examples of significant motions are walking or biking, sitting in a moving car, coach or train, etc. Examples of situations that should not trigger significant motion include phone in pocket and person is not moving, phone is on a table and the table shakes a bit due to nearby traffic or washing machine. For more information, please refer to Android Sensor types: https://source.android.com/devices/sensors/sensor-types.html#significant_motion.

Significant motion function would be triggered by means of monitoring the slope of acceleration over a period of time. The algorithm will be started when a motion is detected, and generates a signal if another motion is detected after the SKIP_TIME[8:0] (0x29-0x2A) and within the PROOF_TIME[7:0] (0x2B). Both 1 LSB of skip time and proof time correspond to 20ms.

The significant motion and slope detection share event-triggered settings including independent XYZ-axes slope enable bit INTEN1 [2:0] (0x16), threshold SLOPETHD [7:0] (0x28), duration SLOPEDLY [1:0] (0x27). User should be noticed that the slope detection has to be enabled before enabling significant motion due to a sharing algorithm engine. Then enable significant motion by writing '1' to SIG_MOT_EN bit in register SIGMOT2 (0x2A).

Follow the steps below to enable significant motion:

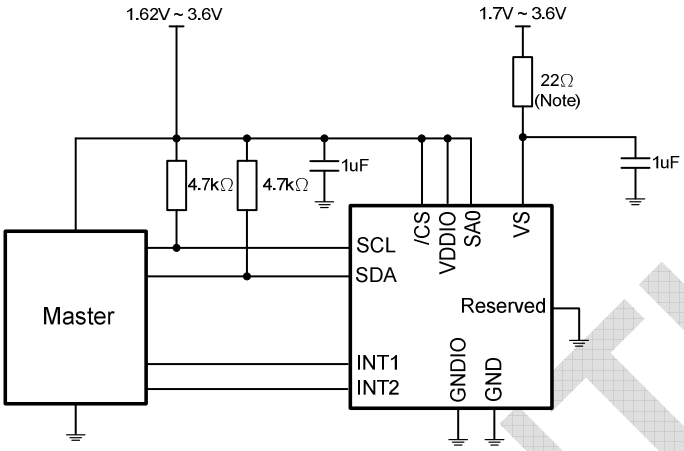
Step1. Set configuration settings include SKIP_TIME[8:0] (0x29-0x2A), PROOF_TIME[7:0] (0x2B), SLOPEDLY[1:0] (0x27) and SLOPETHD[7:0] (0x28).
Step2. Set XYZ-axes slope detection enabled by INTEN1[2:0] (0x16).
Step3. Set significant motion enabled by SIGMOT2[1] (0x2A).
Step4. Mapping significant motion to physical interrupt pin by INTMAP1[0] (0x19).
Step5. Wait for INT triggered or monitor SIG_MOT_STS bit in INTSTS1[0] (0x09)



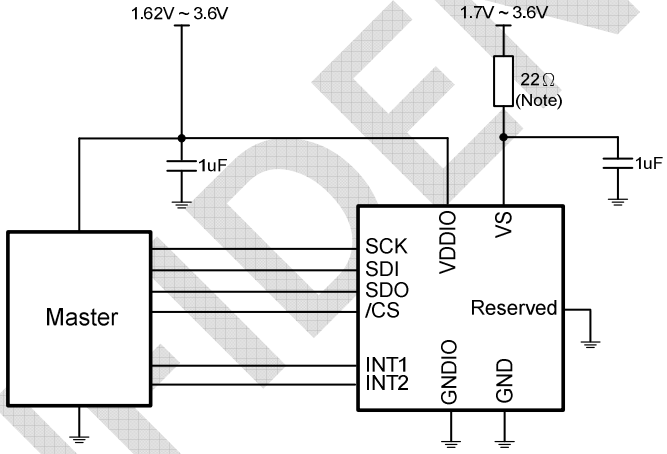
Significant Motion algorithm flow chart

10.4 Application Circuit

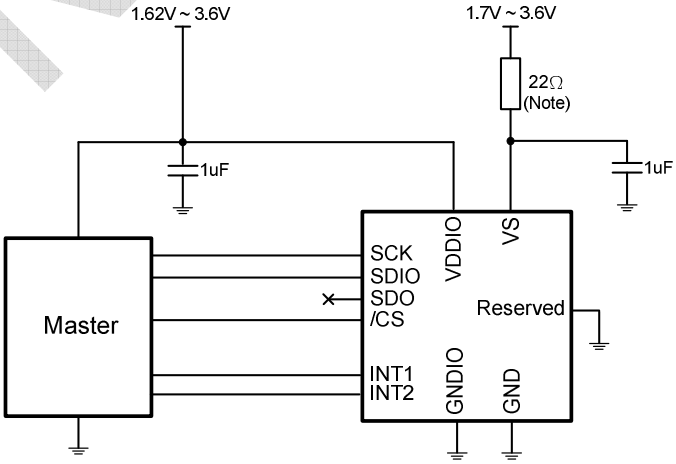
I²C Interface



SPI 4-wire Interface



SPI 3-wire Interface



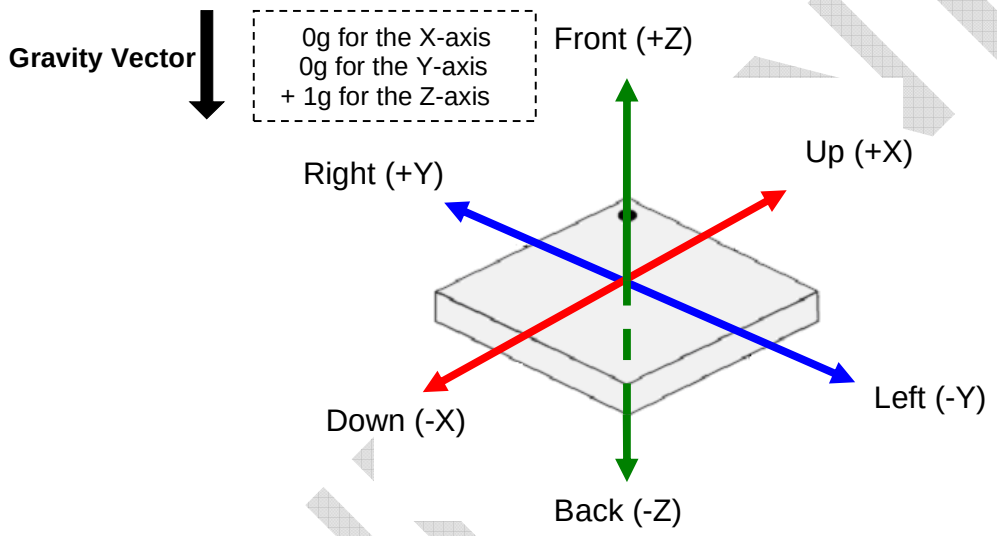
Note: A 22 ohm resistor is recommended to filter out the system power noise.

10.5 Sensing Axes Orientation

By measuring the acceleration components respect to g field, the position and orientation information could be recognized. It could be used for such applications as Portrait/Landscape in Mobile phone/PDA/PMP. This enables a product to set its display orientation appropriately to either portrait/landscape mode, or to turn off the display if the product is placed upside down. The sensor provides positive or negative directions of X/Y/Z axes. The relationship between directions and six different positions: Left, Right, Up, Down, Back, and Front, is shown in the following figure.

If the sensor is at rest and the force of gravity is acting along the indicated directions, the output of the corresponding channel will be negative (static acceleration).

Example: If the sensor is at rest or at uniform motion in a gravity field according to the figure given below, the output signals are:



Sensing axes orientation

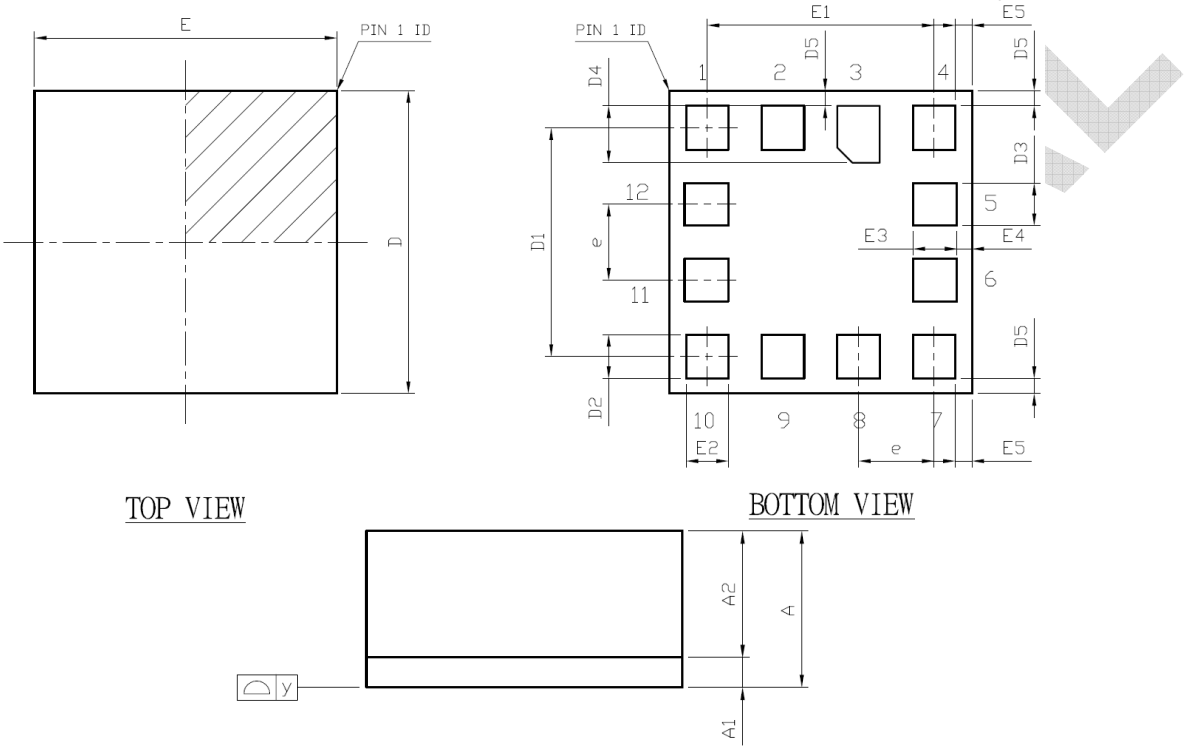
The following table lists all corresponding output signals on X, Y, and Z while the sensor is at rest or at uniform motion in a gravity field under assumption of a ±2g range setting, a 12 bit resolution, and a top down gravity vector as shown above.

Sensor Orientation & Gravity Vector	Top View	Top View	Top View	Top View	Side View	Side View
X-axis Output	+1g/1024LSB	0g / 0 LSB	-1g/-1024LSB	0g / 0 LSB	0g / 0 LSB	0g / 0 LSB
Y-axis Output	0g / 0 LSB	+1g/1024LSB	0g / 0 LSB	-1g/-1024LSB	0g / 0 LSB	0g / 0 LSB
Z-axis Output	0g / 0 LSB	0g / 0 LSB	0g / 0 LSB	0g / 0 LSB	+1g/1024LSB	-1g/-1024LSB

11. PACKAGE OUTLINE

11.1 Package Outline Drawing

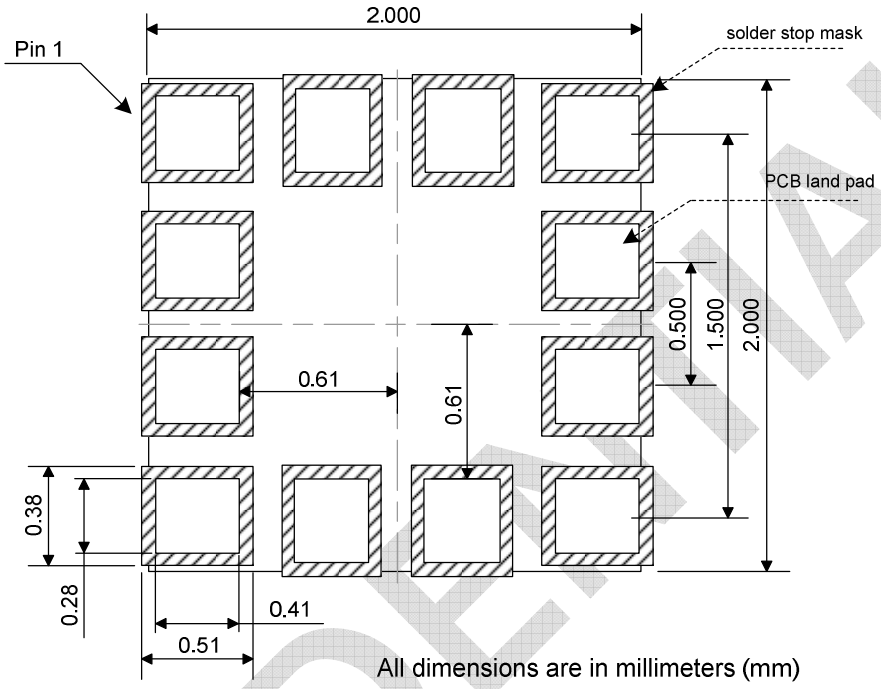
The sensor housing is a 12-pin 2.0mm x 2.0mm x 1.0mm LGA package. Its dimensions are the following.



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX
A	0.95	1.00	1.05
A1	0.16	0.19	0.22
A2		0.80 REF.	
D	1.95	2.00	2.05
D1		1.51 REF.	
D2	0.24	0.29	0.34
D3	0.23	0.28	0.33
D4	0.325	0.375	0.425
D5		0.10 REF.	
E	1.95	2.00	2.05
E1		1.50 REF.	
E2	0.23	0.28	0.33
E3	0.24	0.29	0.34
E4		0.10 REF.	
E5		0.11 REF.	
e		0.50 REF.	
y	0.00	---	0.10

11.2 Recommended PCB Layout

The PCB layout should use NSMD (Non Solder mask Defined) pad definitions for all pads.

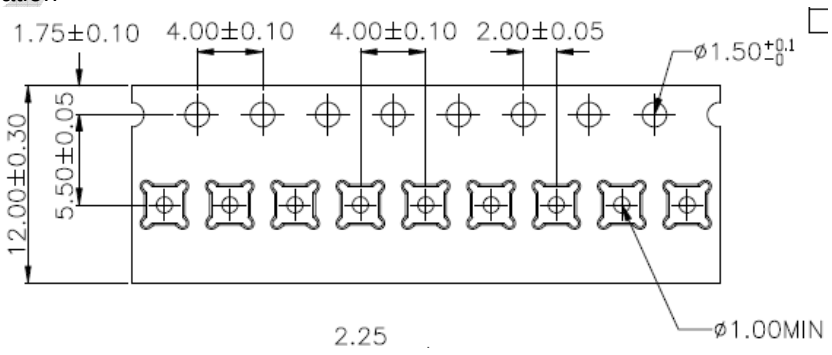


11.3 Marking Rule

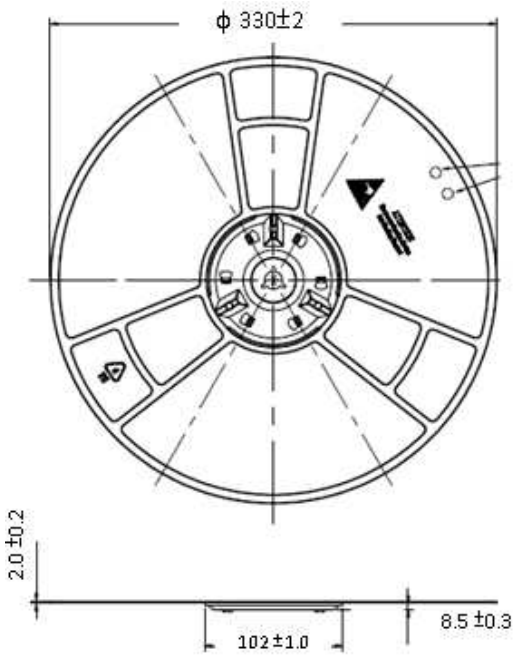
Marking	Symbol	Name
YYYY XXXX ●	YYYY	Order number
	XXXX	Product serial number
	●	Pin1 dot

11.4 Tape and Reel Information

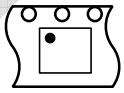
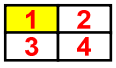
1. Carrier Tape Specification



2. Reel Specification

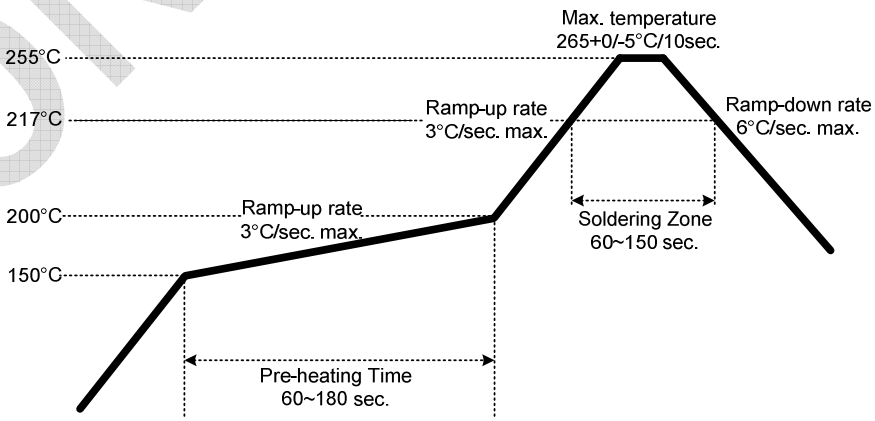


3. Unit Orientation

Process direction	
Orientation in carrier	
Orientation by quadrant	

11.5 Soldering Condition

1. Pb-free solder temperature profile



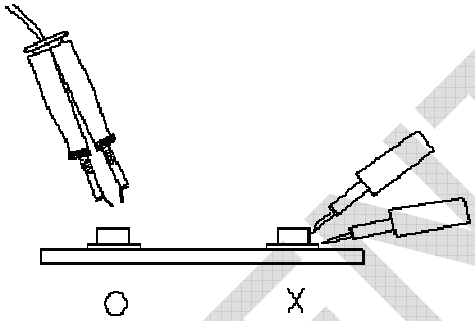
2. Reflow soldering should not be done more than three times.
3. When soldering, do not put stress on the ICs during heating.
4. After soldering, do not warp the circuit board.

11.6 Soldering Iron

Each terminal is to go to the tip of soldering iron temperature less than 350℃ for 3 seconds within once in less than the soldering iron capacity 25W. Leave two seconds and more intervals, and do soldering of each terminal. Be careful because the damage of the product is often started at the time of the hand solder.

11.7 Repairing

Repair should not be done after the ICs have been soldered. When repairing is unavoidable, a double-head soldering iron should be used (as below figure). It should be confirmed beforehand whether the characteristics of the ICs will or will not be damaged by repairing.



12. STORAGE INFORMATION

12.1 Storage Condition

1. Devices are packed in moisture barrier bags (MBB) to prevent the products from moisture absorption during transportation and storage. Each bag contains a desiccant.
2. The delivery product should be stored with the conditions shown below:

Storage Temperature	10 to 30℃
Relatively Humidity	below 60%RH

12.2 Treatment After Unsealed

1. Floor life (time between soldering and removing from MBB) must not exceed the time shown below:

Floor Life	168 Hours
Storage Temperature	10 to 30℃
Relatively Humidity	below 60%RH

2. When the floor life limits have been exceeded or the devices are not stored in dry conditions, they must be re-baked before reflow to prevent damage to the devices. The recommended conditions are shown below

Temperature	60℃
Re-Baking Time	12 Hours

Revision History

Date	Version	Modified Items
2019/08/22	1.0	Initial release.
2020/02/07	1.1	1. Fix sign bit in the sensing axes orientation table.
2020/04/28	1.2	1. Update SPI timing. 2. Fix Typo.
2020/11/17	1.3	1. Update SPI timing chart.
2020/11/25	1.4	1. Update SPI timing spec.
2022/02/10	1.5	1. Update SPI timing spec. 2. Update mechanical specifications.

